PVP 20

Code: 20EE4501E

III B.Tech - I Semester –Supplementary Examinations
NOVEMBER 2023

COMPUTER ORGANIZATION & ARCHITECTURE
(ELECTRICAL & ELECTRONICS ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

		UNIT – I	
1.	a)	Explain Shift Micro-operations with a neat diagram.	10 M
	b)	Demonstrate the hardware implementation of one stage of a logic circuit	4 M
		OR	
2.	a)	Explain the following with respect to memory transfer i) Memory read ii) Memory write	7 M
	b)	Develop a Bus using Multiplexers.	7 M
		UNIT – II	
3.	a)	Explain in detail about Computer Registers with examples.	7 M
	b)	Explain in detail about Memory Reference Instructions.	7 M
		OR	
4.	a)	Demonstrate the different phases of the instruction cycle, including fetch and decode.	6 M
	b)	Explain the role of input-output instructions in	8 M

		computer organization. How are these instructions used to manage data transfer between the CPU and external devices?	
		UNIT-III	
5.	a)	What is the significance of program control instructions in the context of CPU operation? How do they affect the flow of a program?	8 M
	b)	Illustrate the examples of data manipulation instructions and explain their role in arithmetic and logical operations.	6 M
		OR	
6.	a)	Demonstrate various addressing modes used in CPU instruction sets. Provide examples.	8 M
	b)	Compare and contrast the Register Stack and Memory Stack. What are their advantages and disadvantages in different scenarios?	6 M
		UNIT – IV	
7.	a)	Explain Booth's Multiplication Algorithm with an example. How does it work, and what are its advantages in computer arithmetic?	10 M
	b)	Describe the hardware organization of associative memory.	4 M
		OR	
8.	a)	Compare and contrast associative mapping, direct mapping, and set-associative mapping in cache memory organization. What are the trade-offs between these mapping techniques?	8 M

	b)	How associative memory is differ from conventional RAM?	6 M
		UNIT – V	
9.	a)	Analyze the concept of priority interrupt handling. How does daisy-chaining work in a priority interrupt system?	6 M
	b)	Describe asynchronous data transfer in the context of I/O. What are the key elements of asynchronous data transfer, including strobe control and handshaking?	8 M
		OR	
10.	a)	Analyze the working nature of instruction pipe line.	8 M
	b)	Interpret the concept of parallel processing in computer systems.	6 M